Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for testing a ~~memory cell array of a~~ semiconductor memory device ~~in a parallel bit test mode, comprising:~~

~~selecting first data from one of a plurality of memory regions in the memory array for output from the memory device via an input/output pad; and then~~

~~selecting second data from another of the plurality of memory regions for output from the memory device via the input/output pad~~ including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising:

extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to the nm memory cell arrays in a test data write step; and

comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, and outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step.

2. (Currently Amended) The method of Claim 1, wherein ~~selecting first and second data is preceded by reading data from the plurality of memory regions in the memory array~~ in the test data write step, when the x-bit data is written to the respective nm memory cell arrays, the x-bit data written to the nm memory cell arrays are same-bit data.

3. (Currently Amended) The method of Claim 1, wherein ~~the first and second data are both selected from memory regions sharing a row select control line or from memory regions sharing a column select control line~~ the test data read step further comprises:

respectively comparing the x-bit data output from the nm memory cell arrays to generate the nm-bit comparison result data in a comparing step; and

outputting the y-bit comparison result data selected by selecting, by y bits, the nm comparison result data in response to the control signal to the y data I/O pads in a selecting step.

4.-9. (Canceled).

10. (Currently Amended) A method for testing ~~a memory cell array of a semiconductor memory device in a parallel bit test mode, comprising:~~

~~writing test data to a plurality of memory regions in the memory array;~~

~~reading the test data from the plurality of memory regions;~~

~~comparing the test data from the plurality of memory regions to produce comparison data that corresponds to the plurality of memory regions;~~

~~selecting first comparison data corresponding to one of the plurality of memory regions for output from the memory device via an input/output pad; and then~~

~~selecting second comparison data corresponding to another of the plurality of memory regions for output from the memory device via the input/output pad~~ a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising:

extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to the nm memory cell arrays wherein nm is integer time as greater as y in a test data write step; and

comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, grouping and outputting the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal, and outputting y-bit comparison result data generated by respectively comparing the y grouped bit data

through the y data I/O pads in a test data read step.

11. (Currently Amended) A ~~circuit for testing a memory cell array of a~~ semiconductor memory device ~~in a parallel bit test mode~~, comprising:

~~a selecting circuit configured to select first data from one of a plurality of memory regions in the memory array for output from the memory device via an input/output pad, and then select second data from another of the plurality of memory regions for output from the memory device via the input/output pad~~

nm memory cell arrays configured to respectively output x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1;

a test data write circuit configured to extend y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to the nm memory cell arrays; and

a test data read circuit configured to compare the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, and output y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively.

12. (Currently Amended) The ~~circuit~~ device of Claim 11, ~~further comprising a comparator circuit that is configured to read data from the plurality of memory regions and produce comparison data corresponding to the plurality of memory regions, wherein the selecting circuit selects the first and second data from the comparison data~~ wherein in the test data write circuit, when x-bit data is written to the respective nm memory cell arrays, the x-bit data written to the nm memory cell arrays are same-bit data.

13. (Currently Amended) The ~~circuit~~ device of Claim 11, wherein ~~the selecting circuit selects both of the first and second data from memory regions sharing a row select control line or from memory regions sharing a column select control line~~ the test data read circuit includes:

a comparator configured to respectively compare the x-bit data output from the nm memory cell arrays to generate the nm-bit comparison result data; and

a selecting circuit configured to output the y-bit comparison result data selected by selecting, by y bits, the nm comparison result data in response to the control signal to the y data I/O pads.

14.-20. (Canceled).

21. (Currently Amended) A ~~circuit for testing a memory cell array of a~~ semiconductor memory device ~~in a parallel bit test mode~~, comprising:

~~a multiplexer configured to write test data to a plurality of memory regions in the memory array;~~

~~a comparator circuit configured to read the test data from the plurality of memory regions and produce comparison data that corresponds to the plurality of memory regions; and~~

~~a selecting circuit configured to select first comparison data corresponding to one of the plurality of memory regions for output from the memory device via an input/output pad, and then select second comparison data corresponding to another of the plurality of memory regions for output from the memory device via the input/output pad~~

nm memory cell arrays configured to respectively output x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1;

a test data write circuit configured to extend y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to the nm memory cell arrays wherein nm is integer time as greater as y; and

a test data read circuit configured to compare the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, group and output the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a

control signal, and output y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads.

22. – 35. (Canceled).

36. (New) The device of claim 21, wherein in the test data write circuit, when x-bit data are written to the respective nm memory cell arrays, the x-bit data written to the nm memory cell arrays are same-bit data.

37. (New) The device of claim 21, wherein the test data read circuit includes:

a first comparator configured to respectively compare the x-bit data output from each of the nm memory cell arrays;

a selecting circuit configured to group and output the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to the control signal; and

a second comparator configured to output the y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads.

38. (New) The device of claim 37, wherein y is set to at least n when n is greater than m and is set to at least m when m is greater than n.

39. (New) The method of claim 10, wherein in the test data write step, when x-bit data are written to the respective nm memory cell arrays, the x-bit data written to the nm memory cell arrays are same-bit data.

40. (New) The method of claim 39, wherein the test data read step further comprises:

respectively comparing the x-bit data output from each of the nm memory cell arrays in a first comparing step;

grouping and outputting the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal in a selecting step; and

outputting the y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads in a second comparing step.

41. (New) The method of claim 40, wherein y is set to at least n when n is greater than m and is set to at least m when m is greater than n.